Teraflops Research Chip

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Today’s News

• “Tera-scale” computing is coming – supercomputer-like capabilities to PCs, servers and mobile devices

• What we will unveil at ISSCC:
  – Teraflops Research Chip integrating 80 cores – world’s first programmable processor achieving Teraflops of performance with remarkable energy-efficiency
  – Research insights on an innovative tile design methodology, high-bandwidth interconnects and energy management approaches
  – Intel’s tera-scale computing vision – driving compute performance required for more sophisticated and useful software applications
Moore’s Law Motivates Multi-Core

More, better transistors
More cores

Continued benefits from Moore’s Law

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Recent 45nm Breakthrough

- Compared to 65nm, 45nm provides:
  - ~2x improvement in transistor density - smaller chip size or increased transistor count
  - ~30% reduction in transistor switching power
  - >20% improvement in transistor switching speed
  - OR >5x reduction in source-drain leakage power
  - >10x reduction in gate oxide leakage power

45nm will provide the foundation to deliver improved performance/watt, scale multi-core architectures and enhance the user experience.
What is Tera-scale?

Teraflops of performance operating on Terabytes of data

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Intel Tera-scale Research

100+ Research Projects Worldwide

**Microprocessor**
- Examples:
  - Scalable memory
  - Multi-core architectures
  - Specialized cores
  - Scalable fabrics
  - Energy efficient circuits

**Platform**
- Examples:
  - 3D Stacked Memory
  - Cache Hierarchy
  - Virtualization/Partitioning
  - Scaleable OS’s
  - I/O & Networking

**Programming**
- Examples:
  - Speculative Multithreading
  - Transactional memory
  - Workload analysis
  - Compilers & Libraries
  - Tools

**ACCELERATE TRANSITION TO PARALLEL PROGRAMMING**

University Outreach
Intel® Press
Intel® Software College

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A Historical Perspective: ASCI Red

1996: First Teraflops Supercomputer Developed by Intel for Sandia National Lab

- 104 cabinets, over 2500sq feet
- Almost 10,000 Pentium® Pro processors
- Consumed 500kw

Source: Intel, 1996

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Teraflops Research Chip
100 Million Transistors • 80 Tiles • 275mm²

First tera-scale programmable silicon:
- Teraflops performance
- Tile design approach
- On-die mesh network
- Novel clocking
- Power-aware capability
- Supports 3D-memory

Not designed for IA or product
Tiled Design & Mesh Network

Repeated Tile Method:
- Compute + router
- Modular, scalable
- Small design teams
- Short design cycle

Mesh Interconnect:
- “Network-on-a-Chip”
  - Cores networked in a grid allows for super high bandwidth communications in and between cores
- 5-port, 80GB/s* routers
- Low latency (1.25ns*)
- Future: connect IA/or and special purpose cores

* When operating at a nominal speed of 4GHz
Fine Grain Power Management

- Novel, modular clocking scheme saves power over global clock
- New instructions to make any core sleep or wake as apps demand
- Chip Voltage & freq. control (0.7-1.3V, 0-5.8GHz)

Industry leading energy-efficiency of 16 Gigaflops/Watt

Dynamic sleep

STANDBY:
- Memory retains data
- 50% less power/tile

FULL SLEEP:
- Memories fully off
- 80% less power/tile

21 sleep regions per tile (not all shown)

- Data Memory
  - Sleeping: 57% less power
- Instruction Memory
  - Sleeping: 56% less power
- Router
  - Sleeping: 10% less power
    (stays on to pass traffic)
- FP Engine 1
  - Sleeping: 90% less power
- FP Engine 2
  - Sleeping: 90% less power
## Research Data Summary

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Voltage</th>
<th>Power</th>
<th>Bisection Bandwidth</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.16 GHz</td>
<td>0.95 V</td>
<td>62W</td>
<td>1.62 Terabits/s</td>
<td>1.01 Teraflops</td>
</tr>
<tr>
<td>5.1 GHz</td>
<td>1.2 V</td>
<td>175W</td>
<td>2.61 Terabits/s</td>
<td>1.63 Teraflops</td>
</tr>
<tr>
<td>5.7 GHz</td>
<td>1.35 V</td>
<td>265W</td>
<td>2.92 Terabits/s</td>
<td>1.81 Teraflops</td>
</tr>
</tbody>
</table>

1.01 Teraflops  
62 Watts
## Application Performance

At 1.07V, 4.27GHz operation:

<table>
<thead>
<tr>
<th>Application Kernels</th>
<th>FLOP count</th>
<th>Teraflops @ 4.27GHz</th>
<th>% Peak Teraflops</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stencil – PDE Solver</td>
<td>358K</td>
<td>1.00</td>
<td>73.3%</td>
</tr>
<tr>
<td>SGEMM: Matrix Multiplication</td>
<td>2.63M</td>
<td>0.51</td>
<td>37.5%</td>
</tr>
<tr>
<td>Spreadsheet</td>
<td>62.4K</td>
<td>0.45</td>
<td>33.2%</td>
</tr>
<tr>
<td>2D FFT</td>
<td>196K</td>
<td>0.02</td>
<td>2.73%</td>
</tr>
</tbody>
</table>
More than the Cores

- New instructions
- Cache improvements
- HW thread scheduling
- Baseline

Number of cores: 1, 2, 4, 8, 16, 32, 64

Performance increase: 0, 5, 10, 15, 20, 25, 30

Value of Tera-scale Research

Just Adding Cores

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What’s Next?

Many Floating-Point Cores + 3D Stacked Memory

SRAM

Many general-purpose cores

Next research challenge

Research Labs

Product Groups

New Product Development & Design

Future tera-scale processors

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ISSCC: Nine Intel Papers

- "An 80-Tile 1.28TFLOPS Network-on-Chip in 65nm CMOS" - S. Vangal et al.
- Implementation of the 65nm Dual-Core 64b Merom Processor" - N. Sakranet al.
- "A 1.9Gb/s 358mW 16-to-256 State Reconfigurable Viterbi Accelerator in 90nm CMOS" - M. Anders et al.
- "900MHz UHF RFID Reader Transceiver IC" - I. Kipnis et al.
- "A Self-Calibrated On-Chip Phase-Noise-Measurement Circuit with -75dBc Single-Tone Sensitivity at 100kHz Offset" - W. Khalil et al.
- "45% Power Saving in a 0.25μm BiCMOS 10Gb/s 50Ω-Terminated Packaged Active-Load Laser Driver" - E. Ayranci et al.